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Electrical Stability of Hexagonal a-Si:H TFTs

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Abstract
In this paper, we study the current-temperature stress (CTS) induced electrical instability of single and multiple hexagonal (HEX) hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs). The influence of the threshold voltage shift of single HEX-TFT units on the overall electrical performance of multiple HEX-TFTs is discussed. The results indicate that a-Si:H HEX-TFTs have improved electrical stability and good linearity with the number of parallel-connected HEX-TFT units.

1. Introduction
Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) have been extensively used as pixel circuits for large-area flat-panel displays and X-ray imagers due to an excellent spatial uniformity and a low fabrication cost [1-3]. To use such device for active-matrix organic light-emitting diodes (AM-OLEDs) and various analog amplifiers and switches, a higher drain current and better electrical stability under prolonged bias stress are required [4,5]. For a given channel length of standard TFT, a higher drain current can be achieved by increasing the channel width or/and using comb-shaped electrode [6], or fork-shaped electrodes [7]. However, it is well known that a transistor with the increased channel width causes a serious threshold voltage shift (ΔV_{th}) [8]. As an alternative solution, a Corbino a-Si:H TFT has been proposed; the asymmetric ring-shaped electrode make it possible to achieve higher output current and better electrical stability [9]. Due to its circular shape electrodes, unfortunately, it was not easy to increase the channel width or to expand it by connecting Corbino a-Si:H TFTs in parallel.

Hexagonal (HEX) a-Si:H TFT has been successfully demonstrated, and shown unique advantages that can circumvent aforementioned issues: a high output current, an enhanced threshold voltage stability and easy adjustment of current level by connecting a desirable number of HEX-TFTs in parallel [10]. Furthermore, it provides a larger pixel aperture ratio compared to a standard TFT for a given channel width. To evaluate potential of a-Si:H HEX-TFTs connected in parallel for future displays, it is essential to evaluate its individual contribution to the electrical stability of the parallel-connected HEX-TFT. In this paper, we report the detailed study of the current-temperature stress (CTS) induced electrical instability of single and multiple-HEX TFTs. We measured ΔV_{th} of the single and multiple HEX-TFTs at an elevated temperature (80 °C), and then investigated the variation of ΔV_{th} of HEX-TFT units and the influence upon the overall performance of the multiple HEX-TFT.

2. Experiments
Inverted stagger a-Si:H HEX-TFTs were fabricated with a five photo-mask process used in the processing of the active-matrix liquid crystal displays. All multiple HEX-TFT was based on identical single HEX-TFTs. Gate, drain and source electrodes are connected in parallel, respectively (Fig. 1). Detailed process steps can be found in previous publication [10].

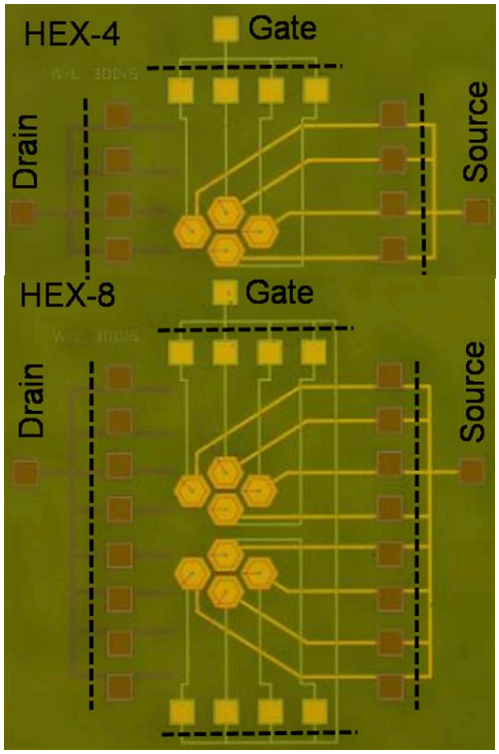

Figure 1. Photographs of HEX-4 and HEX-8 TFTs. Drain bias is applied to inner electrode, and source bias to outer electrode. Dash-lines show the cutting lines.

A series of CTS measurement of the multiple HEX-TFTs were performed by using a semiconductor parameter analyzer (HP 4156A) under an accelerated stress condition by setting the stress temperature at 80 °C [10]. A standard TFT (W/L = 1000/6) was measured as well for comparison. During the CTS, we connected the gate and drain bias (inner-electrode) together and continuously applied the constant current through the drain to the TFT. Source (outer-electrode) of the TFT was grounded. We applied different drain current values depending on the channel width to maintain the same stress current density (1667 A/cm^2) that corresponds to the OLED luminance of 10,000 cd/m^2 for the emission efficiency of 3.0 cd/A and the pixel size of 300 x 100 μm^2 [10]. For example, current of 50, 100 and 167 μA were applied to HEX-1 (W/L = 300/5), HEX-2 (W/L = 600/5) and standard (W/L = 1000/6) a-Si:H TFTs, respectively. The stress time was 10,000 sec, and we only interrupted the stress for 60 sec to measure the transfer characteristics.

Using the same condition, we also measured independently all

single HEX-TFT units by cutting the parallel connection lines (Fig. 1). We performed a thermal annealing at 200 °C for 2 hour to ensure the consistent initial properties of the HEX-TFT units after the CTS measurement of the multiple HEXs. Figure 2 shows that the CTS induced stress could be recovered after the thermal annealing. Then we conducted the CTS measurement for each HEX-TFT unit again. Using the effective channel width calculated by *H.Lee et al.* [10], we extracted the threshold voltages using the maximum slope method [11].

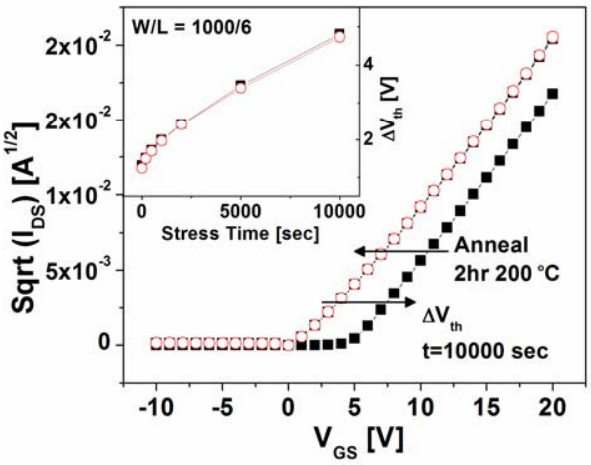

Figure 2. The recovery of the CTS induced stress after thermal annealing. Inset shows the threshold voltage shift (ΔV_{th}) as a function of stress time during CTS experiment. Squares represent the transfer characteristics of the stressed TFT at t = 10000 sec, and circles show it after thermal annealing.

3. Results and Discussions

Figure 3 shows ΔV_{th} of the multiple-HEX TFTs in comparison to the standard TFT over the stress time (10000 sec). ΔV_{th} of HEX-2 (W/L = 600/5), HEX-4 (W/L = 1200/5) and HEX-8 (W/L = 2400/5) are 3.26 V, 3.56 V and 3.82 V, respectively. ΔV_{th} increases with W/L ratio. Similar observation was made by others [8,12]. The larger channel width results in more ΔV_{th} for a given channel length (L = 5 μm). Comparing with the result of the standard TFT (W/L= 1000/6, ΔV_{th} = 3.55 V), we expect that the parallel-connected multiple HEX-TFTs would show better electrical stability for a similar W/L ratio because HEX-4 with even higher W/L ratio shows a similar ΔV_{th} of the standard TFT. Field-effect mobility (μ_{eff}) was also extracted from the transfer characteristics. The amount of μ_{eff} change after CTS for the standard TFT, HEX-2, HEX-4 and HEX-8 are 0.06, 0.07, 0.09 and 0.12 $cm^2/(Vs)$, respectively.

The influence of ΔV_{th} variations of single HEX-TFTs on the overall performance of the multiple HEX-TFTs was also investigated (Fig. 3). ΔV_{th} of all single HEX-TFTs in both HEX-4 and HEX-8 is 3.04 V ± 0.06, which shows a good agreement among the units. No specific single HEX-TFT dominates and affects the overall performance due to a good a-Si:H TFT process spatial uniformity.

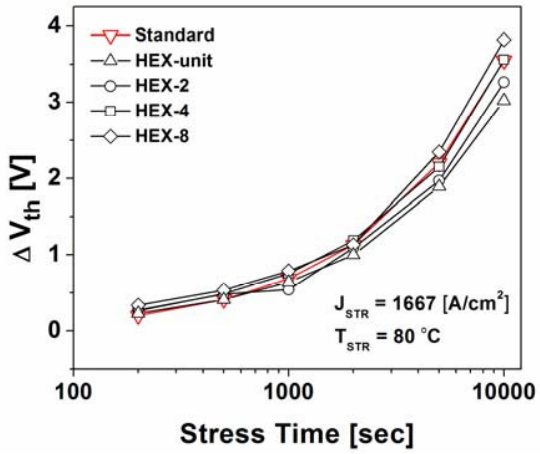

Figure 3. Threshold voltage shifts of the single HEX-TFT units, HEX-2, HEX-4 and HEX-8 TFT. A standard TFT was shown for comparison (squares).

At the low positive bias condition of this experiment, ΔV_{th} is dominated by defect state creation, and so ΔV_{th} is proportional to the total channel charge concentration [13]. As the total channel width increases with the number of parallel-connected HEX-TFTs, channel charges and therefore ΔV_{th} increase. We can expect that parallel-connected multiple HEX-TFTs will show similar ΔV_{th} behavior to its basic units, and the amount of ΔV_{th} of HEX-2^N TFT (N, integer) can be foreseen by adding about 0.27 V x N to ΔV_{th} of the unit HEX-TFT (Fig. 4).

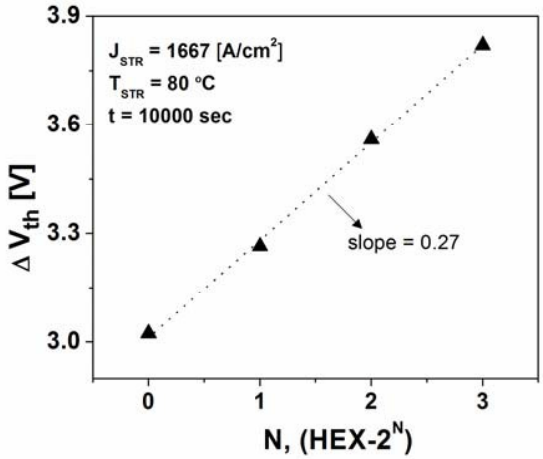

Figure 4. ΔV_{th} as a function of integer, N of HEX-2^N for CTS measurement.

4. Conclusion

In this paper, we studied electrical instability of single and multiple a-Si:H HEX-TFTs under the current-temperature stress. The parallel-connected multiple HEX-TFTs show better electrical stability compared to the standard TFT. It is also found that one specific HEX unit in the multiple HEX-TFT does not affect the

overall electrical stability. This result can be expected from a good a-Si:H TFT process control. Furthermore, we can estimate the threshold voltage shift of the multiple HEX-TFTs based on their HEX-TFT units. Enhanced electrical stability and a good linearity with the number of parallel-connected HEX-TFTs are promising characteristics for the pixel switches to be used in flat-panel displays.

5. Acknowledgements

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